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(54) Frequency synthesisers

(57) The frequency synthesizer shown in Figure 1 comprises a VCO (10), a phase detector (12) which receives a base frequency signal and a feedback signal derived from the output of the VCO (10) and a filter circuit (13) connecting the output of the phase-detector (12) to the frequency control voltage input of the VCO (10). A speed-up circuit (15) is provided for applying a voltage signal to a reference voltage connection (13a) of the filter circuit when a frequency change is demanded. The output of the speed up circuit is applied to the connection (13a) via a capacitor (21) so that the effect of the speed up circuit is temporary. The speed-up circuit may include a plurality of switches 18,19 for applying a selected voltage. Alternatively a D/A converter may apply a voltage dependent on a digital input.

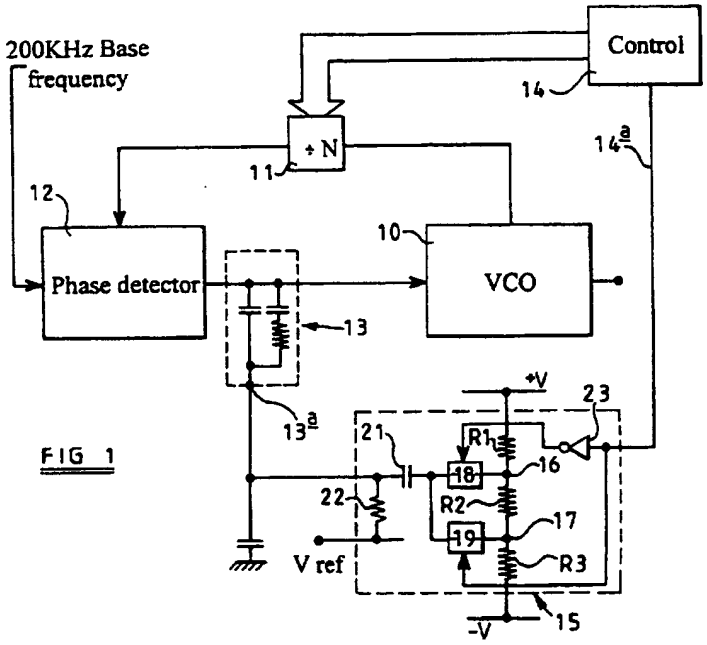

FIG 1

GB 2 317 279 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FREQUENCY SYNTHESISERS

This invention relates to a frequency synthesiser for use, for example, in a communications receiver or transmitter such as a digital telephone.

A GSM telephone, for example, may make use of a frequency synthesiser for switching between receive and transmit frequencies or for frequency hopping during either transmission or receiving. Such a frequency synthesiser will be required to hop over a 70 MHz bandwidth within one GSM time-slot (570 μS). This is difficult to achieve as the loop bandwidth of the synthesiser needs to be kept to a minimum to maintain a low r.m.s. phase noise level.

Previous attempts have been made to speed up locking of the synthesiser loop by either temporarily widening the band width of the synthesiser loop or a voltage steering technique in which an external voltage is applied to the voltage input terminal of a vco used in the synthesiser to drive the vco frequency quickly to a value close to the required frequency. These prior proposals have, however, not been entirely successful, as they involve the introduction of additional active components (operational amplifier, voltage controlled amplifiers or others) inside the synthesiser loop.

It is an object of the present invention to provide a frequency synthesiser with a lock speed-up arrangement in a simple and effective form.

In accordance with the invention there is provided a frequency synthesiser including a voltage controlled oscillator, a phase detector

which receives a base frequency signal and a feedback signal derived from the output of the voltage controlled oscillator and a filter circuit connecting the output of phase detector to a frequency control voltage input of the voltage controlled oscillator, the filter circuit having a reference voltage connection, and a speed-up circuit for applying a voltage signal to the reference voltage connection when a frequency change is demanded.

In the accompanying drawings:

Figure 1 is a diagram of a simple frequency synthesiser intended for operation at just two frequencies, and

Figure 2 is a diagram showing a modification to the example shown in Figure 1 to enable it to operate at many different frequencies.

In the example of the invention shown in Figure 1 of the drawings, the basic synthesiser loop comprising a voltage controlled oscillator 10, a variable frequency divider 11 providing feedback from the voltage controlled oscillator to a phase detector 12 the output voltage from which is applied by a filter circuit 13 to a frequency control voltage input of the voltage controlled oscillator. A control circuit 14 determines the frequency division ratio of the frequency divider 11.

The frequency synthesiser in accordance with the invention differs from prior frequency synthesisers in that the filter circuit 13, which operates as a narrow bandwidth low pass filter, has a voltage reference connection connected, not to a fixed voltage reference source, but to speed-up circuit 15. The speed-up circuit shown is a simple one intended for use

in a situation in which it is required to switch the voltage controlled oscillator between just two different frequencies. To this end it includes a resistor chain R1, R2 and R3 connected between +V and -V supply busses to provide positive and negative voltage signals at nodes 16 and 17. Two analog switches 18 and 19 connect these nodes to an output line 20 which is connected by a capacitor 21 to the reference voltage connection 13a of the filter circuit. A resistor 22 connects the reference voltage connection 13a to the reference voltage source. An output 14a from the control circuit 14 is used to control the analog switches 18 and 19, one via a logical inverter 23.

In operation, the output 14a is high when one frequency is required and low when the other is required. The output 14a switches between its high and low states at the same time as the control output to the frequency divider 11 is changed. When a change occurs the analog switch 18 or 19 which has been conductive is blocked and the other one becomes conductive. When this occurs the positive or negative voltage signal at the appropriate one of the nodes 16, 17 is added to the reference voltage and immediately changes the voltage applied to the vco input by an amount roughly equal to that needed for the output frequency change required. The loop can then quickly stabilise at the new frequency. The resistor 22 causes the added voltage to decay with time. The time-constant of the capacitor 21 and resistor 22 should be long compared with the filter time constants.

In a more complex embodiment shown in Figure 2, the control unit 14 is arranged to control the frequency divider 11 to provide many different frequencies. In this case the control unit is programmed to produce a signed digital output corresponding to the difference between the old

frequency and the new frequency and the speed-up circuit simply comprises an analog to digital converter 23 with its output connected by the capacitor resistor circuit 21, 22 to the connection 13a.

Th speed-up circuits described above operate without any degradation of the phase noise performance of the synthesiser, because no additional active components are included in the loop. No increase in sideband level would occur because no current is leaked from the loop filter. The circuits are very simple and easy to implement in a practical system. In a mobile phone system the switch from standby operation to normal operation could be made very quickly, thereby enabling the start of synthesiser operation to be delayed and saving battery current.

CLAIMS

1. A frequency synthesiser including a voltage controlled oscillator, a phase detector which receives a base frequency signal and a feedback signal derived from the output of the voltage controlled oscillator and a filter circuit connecting the output of phase detector to a frequency control voltage input of the voltage controlled oscillator, the filter circuit having a reference voltage connection, and a speed-up circuit for applying a voltage signal to the reference voltage connection when a frequency change is demanded.

2. A frequency synthesiser as claimed in Claim 1, in which said speed-up circuit has its output capacitively coupled to the reference voltage connection of the filter circuit and there is a resistor connecting said reference voltage connection of the filter circuit to a reference voltage source.

3. A frequency synthesiser as claimed in Claim 1 or Claim 2, in which said speed-up circuit includes a plurality of analog switch devices controlling the connection of a like number of voltage sources to the output connection of said speed-up circuit.

4. A frequency synthesiser as claimed in Claim 1 or Claim 2, in which said speed-up circuit comprises a digital to analog converter for applying to the output connection of the speed-up circuit a voltage dependent on the value of an input digital signal.

5. A frequency synthesiser as claimed in any preceding claim, further comprising a programmable frequency divider connected to provide said feedback signal to the phase comparator, and a control circuit connected to said frequency divider to control the frequency division ratio of the frequency divider, said control circuit also providing a control signal to said speed-up circuit.

6. A frequency synthesiser substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

7. A frequency synthesiser substantially as hereinbefore described with reference to Figure 1 as modified by Figure 2 of the accompanying drawings.

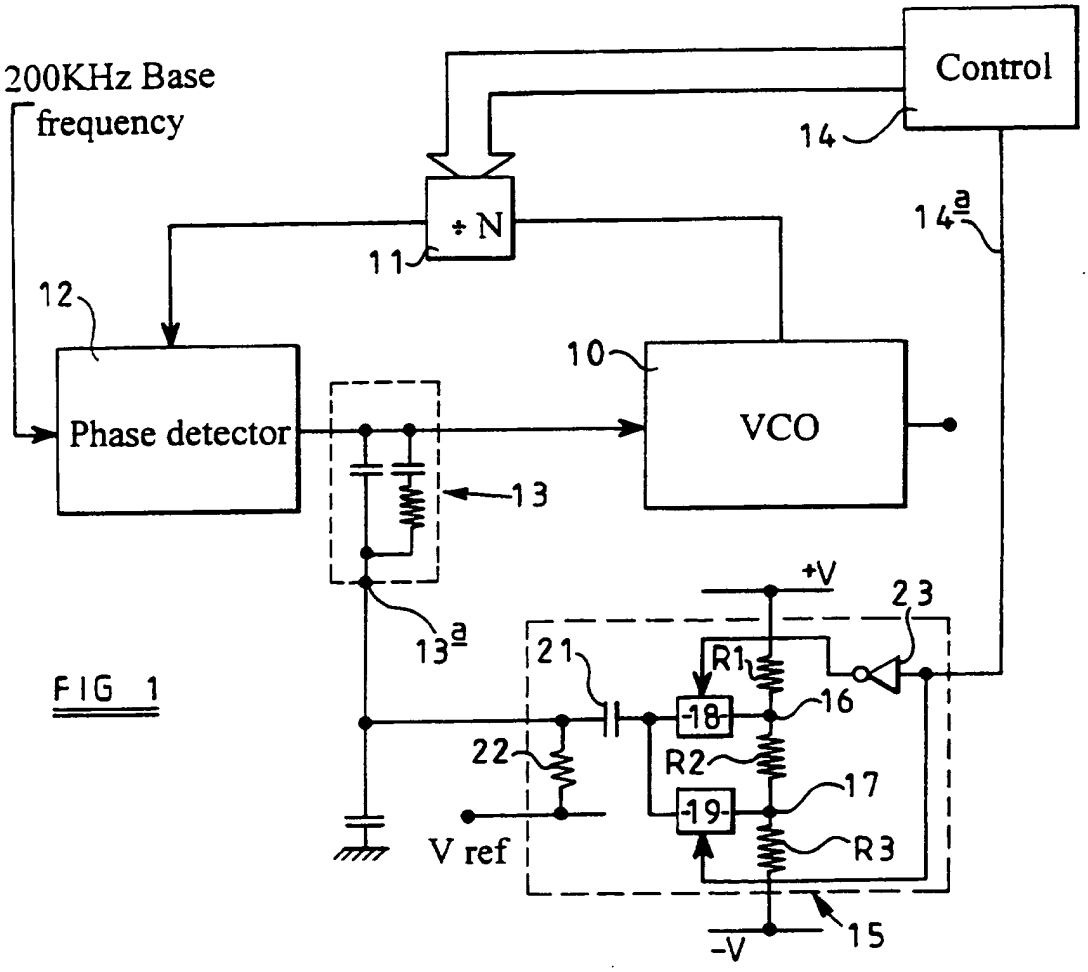

FIG 1

FIG 2